ABSTRACT

0029 A multi-level semiconductor device wiring interconnect structure and method of forming the same to improve electrical properties and reliability of wiring interconnects including an electromigration resistance and electrical resistance, the method including forming a dielectric insulating layer over a conductive portion; forming a via opening in closed communication with the conductive portion; forming a first barrier layer to line the via opening; forming a layer of AlCu according to a sputtering process to fill the via opening to form an AlCu via including a portion overlying the first dielectric insulating layer; and, photolithographically patterning and dry etching the portion to form an AlCu interconnect line over the AlCu via.